REMARKS

The above-referenced patent application has been reviewed in light of the Final Office Action, dated December 1st, 2004, in which: claims 2-5, 7-31 and 43 are rejected under 35 U.S.C 112, second paragraph; claims 2-3, 5, 7-9, 17-18 and 20-24 are rejected under 35 U.S.C 102(e) as being anticipated by *Grisamore* (U.S. Patent No. 6,535,901, hereinafter "*Grisamore*"); claims 4, 10-12, 19 and 25-27 are rejected under 35 U.S.C 103(a) as being obvious over *Grisamore* and in view of Chang et al. (Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs, Nov. 1999, IEEE Computers and Digital Techniques, pages 309-315, hereinafter "*Chang*"); claims 13-16 and 28-31 are rejected under 35 U.S.C 103(a) as being obvious over *Grisamore* in view of *Chang*, and further in view of Fang et al. ("A hierarchical function structuring and partitioning approach for multiple-FPGA implementations, Oct. 1997, IEEE Computer-Aided Design of Integrated Circuits and Systems, pages 1188-1195, hereinafter "*Fang*"); claims 32, 36-38 and 42-43 are rejected under 35 U.S.C 103(a) and being obvious over *Grisamore* in view of Greenberger (U.S. Patent No. 6,411,979, hereinafter "*Greenberger*"); claims 33-35 are rejected under 35 U.S.C 103(a) and being obvious over *Grisamore* in view of *Greenberger*, in view of *Chang*; claims 39-41 are rejected under 35 U.S.C 103(a) and being obvious over *Grisamore* in view of *Greenberger*, in view of *Chang*, and in further view of *Fang*. Reconsideration of the above-referenced patent application in view of the following remarks is respectfully requested. Claims 2-5 and 7-49 are pending in the above-referenced patent application. Claims 2, 5, 17, 20, 32 and 43 have been amended, claims 44-49 have been added and no claims have been canceled.

Applicant's representative conducted an interview with the Examiner's supervisor, Chaki Kakali, on May 27, 2005. The Examiner has rejected claims 2-5, 7-31 and 43 under 35 U.S.C 112, second paragraph, for being indefinite. The Applicant believes the amendments to claims 2, 5, 17, 20 and 43 obviate the rejections, and it is respectfully requested that the Examiner withdraw his rejection of these claims.

Claims 3-4 and 7-16 either depend from or include all the limitations of claims 2 or 5. Therefore, it is respectfully requested that the rejection of these claims be withdrawn. Claims 18-19, 21-31 and 43 are not indefinite for at least the same reasons presented above. It is respectfully requested that the Examiner withdraw his rejection of these claims. The Examiner has rejected claims 2-3, 5, 7-9, 17-18, and 20-24 under 35 U.S.C. 102(e) as being anticipated by *Grisamore*. This rejection by the Examiner is respectfully traversed.

Applicant respectfully submits that *Grisamore* does not disclose each and every element of the rejected claims, and, therefore, a *prima facie* case under 35 U.S.C. 102(e) has not been established. For example, *Grisamore* does not disclose one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results by combining the input terms according to a pipelined reduction pattern. *Grisamore* clearly describes passing partial products to an adder to perform adding functions, and passing and subsequently retrieving carry terms from a memory device. [Col. 2:63-3:8.]

Therefore, applicant respectfully submits that because *Grisamore* does not disclose each and every element of the rejected claims, a *prima facie* case under 35 U.S.C. 102(e) has not been established, and claim 2 is in a condition for allowance. Claim 17 is in a condition for allowance for at least the same reasons as claim 2. Additionally, claims 3, 5, 7-9, 18, and 20-24 either depend from or include all limitations of either claim 2 or 17, and these claims are in a condition for allowance for at least the same reasons as claims 2 and 17.

The Examiner has rejected claims 4, 10-12, 19 and 25-27 under 35 U.S.C 103(a) as being obvious over *Grisamore* and in view of *Chang*, claims 13-16 and 28-31 under 35 U.S.C 103(a) as being obvious over *Grisamore* in view of *Chang*, and further in view of *Fang*, claims 32, 36-38 and 42-43 under 35 U.S.C 103(a) as being obvious over *Grisamore* in view of *Greenberger*, claims 33-35 under 35 U.S.C 103(a) and being obvious over *Grisamore* in view of *Greenberger*, in view of *Chang*, and claims 39-41 under 35 U.S.C 103(a) and being obvious over *Grisamore* in view of *Greenberger*, in view of *Chang*, and in further view of *Fang*.

It is respectfully submitted that *Grisamore* whether viewed alone or in combination with *Chang*, *Fang* and/or *Greenberger*, does not contain all of the elements of the rejected claims. However, Applicant does not by this argument accept that the combination is proper; rather, while Applicant asserts that the combination is improper, Applicant further asserts that even if the combination were proper, the combination would still fail to provide all the elements of the rejected claims.

Applicant begins with claim 4, rejected under 35 U.S.C 103(a) as being obvious over *Grisamore* and in view of *Chang*. The Examiner already concedes that *Grisamore* is lacking one or more elements of the rejected claims. For example, the Examiner states: "*Grisamore* does not disclose the Boolean function generator compris[ing] four-input look-up tables (LUTs) to implement Boolean logic functions. However, Chang et al. disclose[s] in Figure 1(a) Boolean function generator compris[ing] four-input look-up tables (LUTs) to implement Boolean logic functions (left column page 310 lines 1-5.)" However, even if the successful combination of *Grisamore* and *Chang* were made, although, as stated previously, Applicant has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not recite the elements of claim 4. *Chang* is directed generally toward LUT based FPGAs, and does provide the deficiencies of *Grisamore*, noted above. For example, neither *Grisamore* nor *Chang* recite a multi-stage series of Boolean function generators coupled with the inputs to implement one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results.

It is respectfully submitted, therefore, that at least one element of claim 4 is absent from the cited art, and any alleged combination would still not result in a combination having each element of the rejected claim. Therefore, at least one prong of the three-prong test for obviousness has not been satisfied, and a *prima facie* case of obviousness under section 103 of the patent statute has not been made. It is, therefore, respectfully submitted that claim 4 is in condition for allowance.

Claims 10-12, 19 and 25-27 distinguish from the cited art at least on the same basis. It is therefore respectfully requested that the Examiner withdraw his rejection of these claims.

The Examiner has rejected claims 13-16 and 28-31 under 35 U.S.C 103(a) as being obvious over *Grisamore* in view of *Chang*, and further in view of *Fang*. This rejection by the Examiner is also

respectfully traversed. The Examiner already concedes that *Grisamore* is lacking one or more elements of the rejected claims. For example, the Examiner states: "Grisamore does not disclose in Figures 1, 4-5, and 7 a controller or a logic module dynamically structures the atomic elements of the dedicated logic device. However, Fang et al. disclose in Figure 3 a controller or a logic control module dynamically ... structures the atomic elements of the dedicated logic device." However, even if the successful combination of *Grisamore, Chang* and *Fang* were made, although, as stated previously, Applicant has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not recite the elements of the rejected claims. *Fang* is directed toward structuring and partitioning of FPGA implementations. The cited passage recites hierarchical structuring of an FPGA implementation, and does not provide the deficiencies of *Grisamore*, noted above. For example, neither Grisamore, Chang nor *Fang* recite a multi-stage series of Boolean function generators coupled with the inputs to implement one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results.

It is respectfully submitted, therefore, that at least one element of claims 13-16 and 28-31 are absent from the cited art, and any alleged combination would still not result in a combination having each element of the rejected claim. It is, therefore, respectfully submitted that claims 13-16 and 28-31 are in condition for allowance.

The Examiner has rejected claims 32, 36-38, and 42-43 under 35 U.S.C 103(a) as being obvious over *Grisamore* in view of *Greenburger*, claims 33-35 under 35 U.S.C 103(a) as being obvious over *Grisamore* in view of *Greenburger, further in view of Chang, and claims 39-41* under 35 U.S.C 103(a) as being obvious over *Grisamore* in view of *Greenburger*, in further view of Chang, in further view of Fang. Beginning with claim 32, the Examiner already concedes that *Grisamore* is lacking one or more elements of the rejected claims. For example, the Examiner states: "Grisamore does not implicitly disclose two paths one for a real component branch, inverting certain partial produces and passing the inverted and non-inverted partial products and one for an imaginary component branch, passing the partial products to a multi-stage series of Boolean function generators simultaneously." It is

respectfully submitted that even if the successful combination of *Grisamore* with *Greenburger, and/or Chang and/or Fang* were made, although, as stated previously, Applicant has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not recite the elements of the rejected claims. *Greenburger* is directed toward a complex number multiplier circuit, and does not provide the deficiencies of *Grisamore* and/or *Chang* and/or *Fang*, noted above. For example, neither *Grisamore*, *Chang*, *Fang* nor *Greenburger* recite simultaneously passing the partial products from the two or more input terms to a multi-stage series of Boolean function generators that implements one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results by combining the partial products.

It is respectfully submitted, therefore, that at least one element of claim 32 is absent from the cited art, and any alleged combination would still not result in a combination having each element of the rejected claim. Therefore, a *prima facie* case of obviousness under section 103 of the patent statute has not been made. It is, therefore, respectfully submitted that claim 32 is in condition for allowance.

Claims 33-43 depend from and include all limitations of claim 32, and distinguish from the cited art at least on the same basis as claim 32. It is therefore respectfully requested that the Examiner withdraw his rejection of these claims.

Applicants have added new claims 44-49. It is respectfully submitted that there is adequate support in the specification for the new claims, and the new claims do not introduce any new matter. Additionally, it is respectfully submitted that new claims 44-49 are patentable for reasons similar to those presented in support of claims 2-5 and 7-43.

CONCLUSION

In view of the foregoing, it is respectfully submitted that all of the claims pending in this patent application, as amended, are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (503) 640-6475. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Please charge any shortages and credit any overcharges of any fees required for this submission to Deposit Account number 50-3130.

Respectfully submitted,

Dated: 6/1/05

Michael J. Willardson
Patent Attorney
Reg. No. 50,856

Berkeley Law & Technology Group, LLC
5250 NE Elam Young Parkway, Suite 850
Hillsboro, Oregon 97124
503.640.6475